CLAIMS

1-21. (Canceled).

22. (Previously Presented) A method for producing an output pulse, comprising:

receiving an input pulse having a width extending between a start and an end;

starting production of the output pulse responsive to the start of the input pulse;

determining whether the width of the input pulse is greater than a maximum pulse width; and

in the event the width of the input pulse is greater than the maximum pulse width, ending production of the output pulse such that a width of the output pulse is substantially equal to the maximum pulse width.

23. (Previously Presented) The method as recited in claim 22, further comprising:

in the event the width of the input pulse is not greater than the maximum pulse width, ending production of the output pulse responsive to the end of the input pulse such that the width of the output pulse is substantially equal to the width of the input pulse.

24. (Previously Presented) The method as recited in claim 22, wherein the determining is carried out using a time delay element having a delay time that determines the maximum pulse width.

25. (Previously Presented) An apparatus for producing an output pulse, comprising:

means for receiving an input pulse having a width extending between a start and an end;

means for starting production of the output pulse responsive to the start of the input pulse;

means for determining whether the width of the input pulse is greater than a maximum pulse width; and

means for, in the event the width of the input pulse is greater than the maximum pulse width, ending production of the output pulse such that a width of the output pulse is substantially equal to the maximum pulse width.

26. (Previously Presented) The apparatus as recited in claim 25, further comprising:

means for, in the event the width of the input pulse is not greater than the maximum pulse width, ending production of the output pulse responsive to the end of the input pulse such that the width of the output pulse is substantially equal to the width of the input pulse.

27. (Previously Presented) The apparatus as recited in claim 25, wherein the means for determining whether the width of the input pulse is greater than the maximum pulse width comprises a time delay element having a delay time that determines the maximum pulse width.

28. (Previously Presented) The apparatus as recited in claim 25, wherein the apparatus comprises dynamic logic having one or more dynamic nodes.

29. (Previously Presented) A pulse limiting circuit, comprising:

a first logic unit adapted to receive an input signal, including an input pulse, and a first signal, and configured to generate and store a logic value responsive to the input signal and the first signal;

a second logic unit adapted to receive the input signal and the stored logic value, and configured to produce a second signal and an output signal responsive the first signal and the stored logic value;

a time delay element adapted to receive the second signal and configured to produce the first signal dependent upon the second signal and a delay time of the time delay element;

wherein the delay time of the time delay element determines a maximum pulse width; and

wherein the second logic unit produces the output signal such that the output signal comprises an output pulse triggered by the input pulse and having a width that is less than or equal to the maximum pulse width.

30. (Previously Presented) The circuit as recited in claim 29, wherein the input signal is a clock signal including a plurality of pulses in sequence, and the input pulse is one of the plurality of pulses.

31. (Previously Presented) The circuit as recited in claim 29, wherein the first logic unit comprises a pair of cross coupled inverter gates configured to store the logic value.

32. (Previously Presented) The circuit as recited in claim 29, wherein the second logic unit comprises an inverter gate coupled to receive the second signal and producing the output signal.

33. (Previously Presented) The circuit as recited in claim 29, wherein the time delay element comprises a plurality of logic gates coupled in series.

34. (Previously Presented) The circuit as recited in claim 29, wherein the input pulse is a negative going portion of the input signal, and wherein the output pulse is a negative going portion of the output signal.

35. (Previously Presented) The circuit as recited in claim 29, wherein the second logic unit produces the output signal such that the output pulse has a width that is: (i) substantially equal to the width of the input pulse in the event the width of the input pulse is less than or equal to the maximum pulse width, and (ii) substantially equal to the maximum pulse width in the event the width of the input pulse is greater than the maximum pulse width.

36. (Previously Presented) A pulse limiting circuit, comprising:

determining logic adapted to receive an input signal including an input pulse and comprising at least one time delay element, wherein the determining logic is configured to produce either a first signal or a second signal dependent upon a width of the input pulse;

set logic adapted to receive the input signal and to produce a set signal dependent upon the input pulse;

reset logic coupled to receive the first signal and the second signal and configured to logically OR the first and second signals to produce a reset signal; and

a pair of cross-coupled NAND gates, wherein one of the NAND gates is coupled to receive the set signal and configured to produce an output signal, and wherein the other NAND gate is coupled to receive the reset signal;

wherein a delay time of the at least one time delay element of the determining logic determines a maximum pulse width; and

wherein the one of the NAND gates produces the output signal such that the output signal comprises an output pulse triggered by the input pulse and having a width that is less than or equal to the maximum pulse width.

37. (Previously Presented) The pulse limiting circuit as recited in claim 36, wherein the input signal is a clock signal including a plurality of pulses in sequence, and the input pulse is one of the plurality of pulses.

38. (Previously Presented) The pulse limiting circuit as recited in claim 36, wherein the determining logic produces the first signal in the event the width of the input pulse is greater than the maximum pulse width.

39. (Previously Presented) The pulse limiting circuit as recited in claim 36, wherein the determining logic produces the second signal in the event the width of the input pulse is less than or equal to the maximum pulse width.

40. (Previously Presented) The pulse limiting circuit as recited in claim 36, wherein the input pulse is a positive going portion of the input signal, and wherein the output pulse is a positive going portion of the output signal.

41. (Previously Presented) The pulse limiting circuit as recited in claim 36, wherein the one of the NAND gates produces the output signal such that the output pulse has a width that is: (i) substantially equal to the width of the input pulse in the event the width of the input pulse is less than or equal to the maximum pulse width, and (ii) substantially equal to the maximum pulse width in the event the width of the input pulse is greater than the maximum pulse width.